27.6 A 14b 74MS/s CMOS AFE for True High-Definition Camcorders

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Modern video cameras have been trending towards higher resolutions, as high as 1920 × 1080 for high-definition (HD) video, with frame rates up to 60frame/s progressive-scan. In order to support these resolutions and frame rates, the HD standard defines the maximum sampling rate of 74.25MS/s. Figure 27.6.1 shows a block diagram of an example HD camera system. The image is focused through a lens and split with a prism onto three sensors, one each for the red, green, and blue colors. Each channel also has an AFE that conditions, digitizes, and serializes the data, then sending it to the DSP. Since each pixel contains information from all 3 channels, HD video requires a minimum of 3 AFEs, each operating at 74.25MS/s. While there have been high-speed AFEs published [1, 2, 3], none are able to support true HD video formats.

An integrated AFE capable of 74.25MS/s sample rates with 14b resolution for HD camcorders is presented. Integrated in 0.18µm CMOS, the chip operates from a 1.8V supply and employs several high-speed low-power circuit techniques, resulting in low power-per-MS/s. In this paper, several of the circuit techniques used will be described.

As shown in Fig. 27.6.1, all AFE sub-blocks for one color channel are integrated on a single chip. The analog portion of the signal chain consists of a correlated double sample (CDS) amplifier, a VGA, a 14b ADC, and a voltage reference (REF). The AFE also contains a black-level correction loop that removes sensor offsets. Following the AFE are digital functions for signal processing. After digital processing, the data is serialized and output through a 1.2Gb/s serial LVDS interface. Changing from parallel CMOS to serial LVDS outputs improves power dissipation, sensitive high-speed data coupling and EMI. Finally, a timing core uses an external 74.25MHz clock to generate all of the internal timing to 0.2ns precision.

A switched-capacitor amplifier performs the CDS function on the input waveform, as shown in Fig. 27.6.2 along with a sample timing diagram. During the Q1 clock phase, the sensor reset level is sampled onto C_S while an offset voltage is sampled onto C_F. The auto-zero configuration also samples amplifier offset and low-frequency noise onto C_S and C_F. During Q2, the difference between the sampled reset level and the sensor data level is amplified on C_F. Also, the duty cycle of Q1 and Q2 are typically skewed in order to match sensor timing. This duty cycle skew, along with non-overlap timing, leaves about 4.5ns for amplifier settling during the Q2 phase, which is equivalent to a 110MHz half-period.

The CDS amplifier consists of a resistively loaded pre-amplifier followed by a transconductance stage. Instead of a fixed bias, both amplifier stages are biased with current inversely proportional to poly-silicon sheet resistance. These currents are generated by forcing the stable reference voltage across a poly-Si resistor. The overall transconductance of the CDS amplifier is the product of the pre-amp gain and the second stage transconductance, $G_{M1}R_LG_{M2}$. Since G_{M1} and G_{M2} are proportional to the square root of the drain current, the overall transconductance is independent of sheet resistance variation. Thus, no extra power is required under nominal conditions to account for resistor processing variations.

One of the major difficulties in moving towards higher conversion rates is the decreased available settling time, 4.5ns in this design. Amplifiers such as the push-pull topology shown in Fig. 27.6.3 can efficiently achieve high-speed settling while driving large capacitive loads. In conventional designs [4], linear behavior dominates amplifier settling. Due to higher f_T transistors in deep sub-micron CMOS, slew behavior can dominate. The advantage of push-pull amplifiers is the availability of large transient current while consuming small standing current. Also, switched-capacitor level-shifting allows direct coupling between the first and second stages [5]. Compared to active level-shifting, switched-capacitor level-shifting is power efficient and minimizes parasitic poles. Also, the amplifier is able to operate in both clock phases due to the use of charge refresh capacitors C_{REF} to bias C_{LS}. The push-pull topology is used in amplifiers throughout the AFE, for example allowing a 38% power reduction in the ADC first stage amplifier.

The ADC is a 3b front-end, followed by a scaled 1.5b/stage pipeline that is efficient for achieving low-power 14b linearity without calibration [4]. Another low-power circuit technique used is amplifier sharing [6]. Shown in Fig. 27.6.4, it uses the same amplifier to generate the residue signals for both stages N and N+1. In phase 1, the output of stage N-1 is sampled onto C_N while the amplifier is driving the N+1 residue signal into stage N+2. In phase 2, the amplifier drives the N residue signal onto C_{N+1}. The sub-flashes are not shown. Due to practical considerations, such as bandwidth reduction due added capacitance on the summing nodes, the power reduction from sharing is <50%. In this AFE, the ADC back-end uses sharing, reducing power by 33%.

The complete AFE is integrated in 0.18µm 1P5M CMOS with MIM capacitors. Figure 27.6.5 shows the measured non-linearity or error expressed as a percent of output level, and DNL. The non-linearity is reported for a 1V full-scale input with 6dB gain. At black level with 3dB gain, the peak SNR is 78dB. The power dissipation from a single 1.8V supply is 70mW for the analog portion of the chip, corresponding to a power-per-MS/s of 0.95mW-per-MS/s. Figure 27.6.6 shows the AFE response to a full-scale step input at 74.25MS/s. The step response shows that the AFE has the bandwidth required for 1% settling in 1 pixel, 0.1% in 2 pixels.

References:

[1] K. Nakamura, et al., "A CMOS Analog Front-End Chip-Set for Mega Pixel Camcorders," *ISSCC Dig. Tech. Papers*, pp. 190-191, Feb., 2000.
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[3] B. Ahuja, et al., "A 30Msample/s 12b 110mW Video Analog Front End for Digital Camera," *ISSCC Dig. Tech. Papers*, pp. 438-439, Feb., 2002.
[4] D. Kelly, et al., "A 3V 340mW 14b 75MSPS CMOS ADC with 85dB SFDR at Nyquist," *ISSCC Dig. Tech. Papers*, pp. 134-135, Feb., 2001.
[5] P. Allen, P. and D. Holberg, "CMOS Analog Circuit Design," 1st Edition, Holt, Rinehart, and Winston, 1987, pp. 509-511.
[6] K. Nagaraj, et al., "A 250-mW, 8-b, 52-Msample/s Parallel-Pipelined A/D Converter with Reduced Number of Amplifiers," *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 312-320, Mar., 1997.

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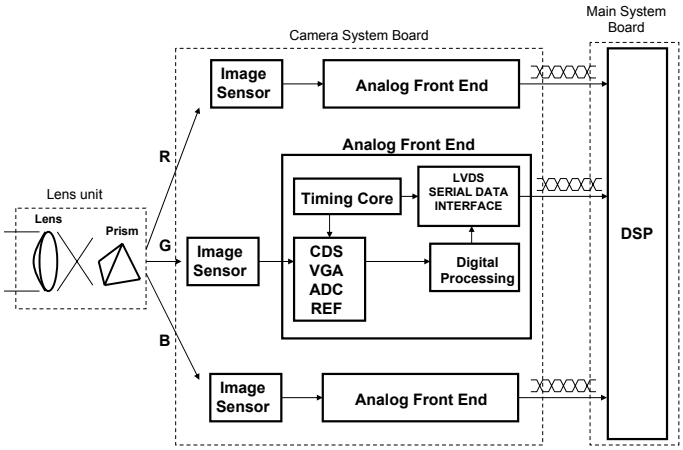

Figure 27.6.1: Example HD camera system.

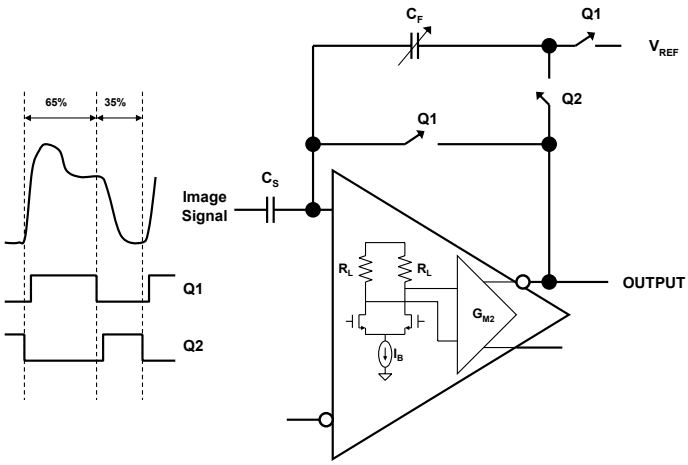

Figure 27.6.2: CDS implementation.

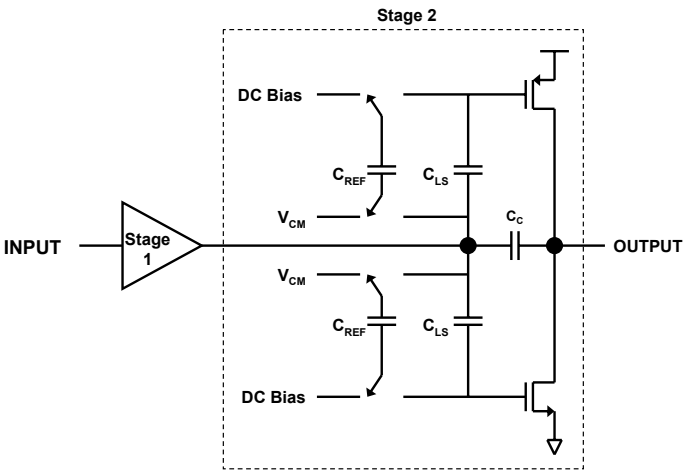

Figure 27.6.3: Push-pull amplifier.

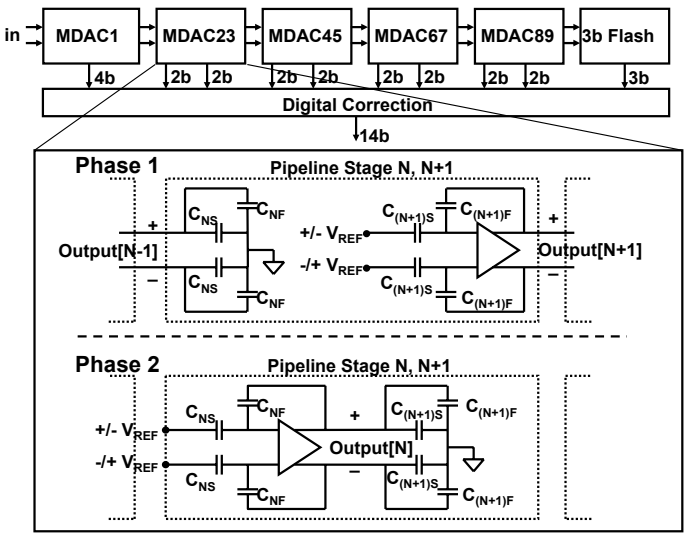

Figure 27.6.4: 14b ADC and amplifier sharing.

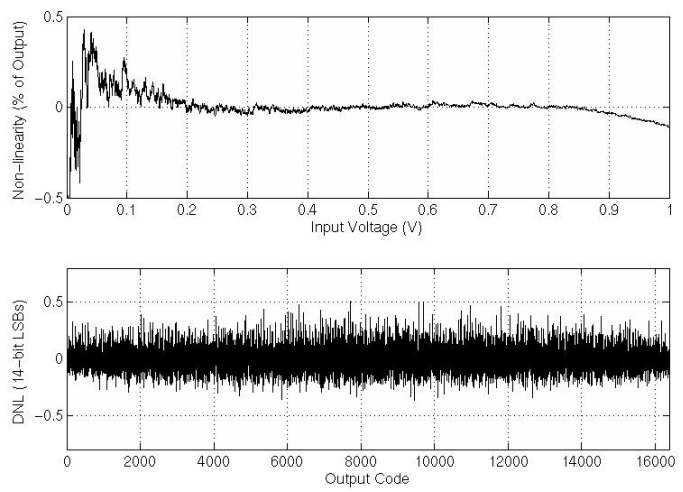

Figure 27.6.5: Non-linearity and DNL.

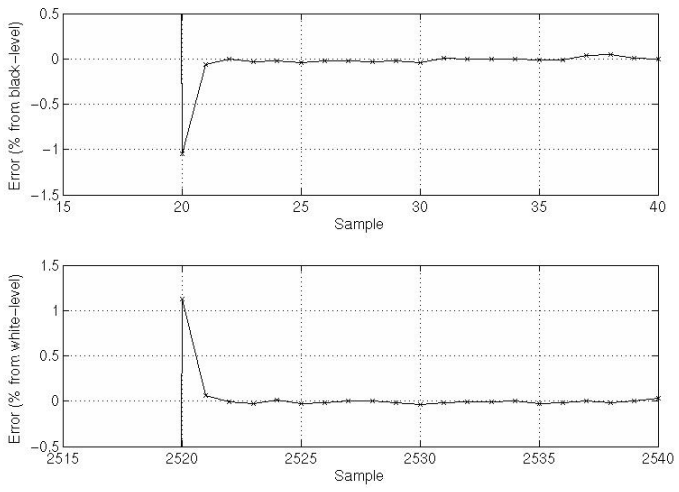

Figure 27.6.6: Step response.